Amendments to the Specification

Please amend the paragraph beginning on page 18, line 13 as follows:

A layer of poly-silicon 466 is then deposited over the entire structure (Fig. 28). The poly-silicon layer 466 can, for example, for formed to about 2400 to 5000 Angstroms. It will be appreciated that some of the poly-silicon 466 fills in the void 464 created over the N-type surface layer 442 of the DWELL 430 during patterning of the oxide layer 460. The layer of poly-silicon 466 is then patterned so as to serve as part of a gate electrode stack 502 of a CMOS/DMOS device 500 (Fig. 29). It will be appreciated that the poly-silicon 466 may include a dopant, such as a P-type dopant (*e.g.*, Boron) or may be subsequently doped.

Please amend the paragraph beginning on page 18 line 20 as follows:

One or more subsequent implants 470 (such as those employed in the BiCMOS process to form P-type and N-type source/drain regions) are then performed to form a collector region contact and a base region contact, respectively (Fig. 30). Accordingly, a PMOS source/drain mask (not shown) may be utilized to define an opening through which a P-type source/drain implant 470 is performed to form a PSD (P-type source/drain) region 472 that serves as a contact for the collector region of the poly-emitter vertical bipolar transistor. Such implant may also be used to dope the poly-silicon emitter contact 466. Similarly, an NMOS source/drain mask (not shown) may be employed to define one or more openings through which an N-type source/drain implant 470 is performed to form an NSD (N-type source/drain) region(s) 474 that serves as a contact for the base of the bipolar transistor 400. That is, the same implant 470 employed to form the PMOS and NMOS transistor source/drain regions 504 elsewhere on the semiconductor wafer die is employed to form the collector contact and base contact for the bipolar transistor 400.